## OPERATION OF A COUNTER CIRCUIT

Last of a Five Part Article submitted by Herbert Grossman, FSDM, New Hyde Park, New York

A counter is composed of cascaded flip-flop stages. Each flip-flop uses a one-diode gate on the reset side and a two diode gate on the set side.

Each flip-flop stage depends on its previous stage for operation. The flip-flops in the counter are designated as $2^{0}, 2^{1}, 2^{2}$, etc.

The voltage normally appearing on the " 1 " or set side of a "set" flip-flop is zero, while that on the corresponding "reset" side is -6.0 volts, depending on whether the flip-flop has been "set" or "reset".

Figure 1 shows the schematic of a 4 stage counter. Figure 2 is the logic diagram of this 4 stage counter.

The counter shown has two conditions for each flip-flop, either "set" (" 1 ") or "reset" (" 0 ") zero. In all, there are four flip-flops which would give 16 different combinations of settings.

Figure 2 shows the various combinations with respect to the number of pulses the counter has counted. The trigger input will advance the counter by one for each pulse received and all counters use a positive going pulse input. The start pulse is applied to all stages of the counter to reset the counter to the zero state. This insures that no residual count is in the counter when the counting operation begins.

The positive going pulse is capacity coupled into the first stage of the counter with both bases receiving the pulse simultaneously. This method of coupling will cut off the conducting transistor and have little effect on the other transistor. Since the use time is short compared to the switching time of the flip-flop, the system will change its state. The flip-flop will therefore change its state with every input pulse. The output of the first stage (Q1 and Q2) is coupled to the input of the second through a diode gate. This gate will permit only the positive portion of the differentiated output of the first stage to pass. The second stage therefore changes state only when a
positive rise in the collector of Q1 is realized. This stage changes state one-half as many times as the tirst stage, or divides the output of the first stage by two.

The successive flip-flop stages are connected to the previous stages in the same manner as the one described. Since each successive stage will change state one-half the number of times the previous stage changes its state, a binary counter results. The maximum count available is $2^{\mathrm{N}}-1$ where N is equal to the number of stages.

When the first trigger pulse arrives at the trigger input, it will attempt to pass through CR4 and CR5. Due to the negative voltage from the collector of Q1 on CR4 anode, the pulse cannot pass through CR4, while diode CR5 allows the positive pulse to pass and cut off Q2.

The collector of Q1 changes from - 6 volts to zero volts; this produces a positive going pulse, which is applied to CR9 and CR10. Because of the negative inhibiting level from Q3 collector, the positive pulse can only pass through CR10. Diode CR10 conducts and Q4 cuts off and Q3 starts to conduct. This procedure is followed through the entire counter. The counter (due to the first pulse received) will be changed from an all "one" to an all "zero" state. The second pulse arrives at the trigger input and cuts off Q1. The negative pulse that is formed on Q1 collector will not affect the following stage. The counter will advance in the manner described. Figure 2 shows the particular configuration for each binary count of the counter related to the data interval it represents. When the "set" side of a flip-flop is going from a " 1 " to a " 0 " then the following stage will change its condition.

When a counter is first turned on, or a particular operation has been completed, the counters will be at some random count. In order to insert new information, it is necessary to clear the counter. This is accomplished by placing a positive level at the common set level input which will drive all the reset sides of the flip-flops to cut off. The counter will then be in all "ones" (or "set") condition.



CONDITION OF STAGES AFTER:

| Start pulse |  | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PULSE \# |  | 1 | 0 | 0 | 0 |
| " |  | 0 | 1 | 0 | 0 |
| " |  | 1 | 1 | 0 | 0 |
| " | 4 | 0 | 0 | 1 | 0 |
| " |  | 1 | 0 | 1 | 0 |
| " |  | 0 | 1 | 1 | 0 |
| " | 7 | 1 | 1 | 1 | 0 |
| " |  | 0 | 0 | 0 | 1 |
| " |  | 1 | 0 | 0 | 1 |
| " | 10 | 0 | 1 | 0 | 1 |
| " | 11 | 1 | 1 | 0 | 1 |
| " | 12 | 0 | 0 | 1 | 1 |
| " |  | 1 | 0 | 1 | 1 |
| " | 14 | 0 | 1 | 1 | 1 |
| " |  | 1 | 1 | 1 | 1 |

WAVE FORMS:
START PULSE $\quad]$
INPUT PULSES


$$
2^{3}(1)
$$

Figure 2

## PESSIMIST SOUNDS OFF

Summer again!
Yes, summer begins June 21. But beware! The activities of those beautiful sunny days can be dangerous.

How? Consider . . .
The barbeque. Fumes from charcoal are reported to be carcinogenic - cancer inciting. Why take a chance?

Swimming. More people drown in the summer than any other time of the year, and many beach areas are polluted. Better not swim.

Picnicking. That potato salad and tuna sandwich made with mayonnaise can cause salmonella if those foods are not properly refrigerated. Do you have to picnic? And think of the cholesterol content as well as the cost of steaks and hamburgers. Stick to celery and carrots.

Sunbathing. Too much sun can dry out your skin and make it look leathery, old. More important, why risk the chance of skin cancer? Better keep out of the sun.

Cold soft drinks. Nothing like something icy and wet on a hot day. But prepare for cramps and think of the caloric intake. Rely on tap water at faucet temperature.

Boating. Like swimming, boating is dangerous, for any body of water can mean another drowning. Wouldn't you be safer at home?

Vacationing, in general. Think of the new germs waiting to attack you when you are far from home. And give some thought to the changes in temperature, sleeping accomodations, and drinking water. These alone are enough to make you ill. Shouldn't you stay at home?

So watch how and what you eat, where you swim, how much you sun, and why you vacation... AND have a happy summer!

## NOTES FROM THE FIELD

D1905 CHASSIS. VERTICAL FOLD @ BOTTOM.
Intermittent 27 V winding on power transformer.
Adrian Jasonski, Sun T. V. \& Appliance, Columbus, Ohio.
E03 CHASSIS. POOR COLOR SYNC.
Open R524, 8.2K on IF panel.
E03 CHASSIS. INSUFFICIENT VERTICAL SWEEP.
R362, 15 ohms, 3 W , reads 400 ohms.

E03 CHASSIS. LOW BRIGHTNESS - LOOKS LIKE BAD CRT.
Shorted SC445 Boost diode.
E03 CHASSIS. NO SOUND, NO PIX (DEAD).
Power Transformer T500 open primary.
E03 CHASSIS. NO VERTICAL SWEEP.
Shorted SC355 and Shorted Q306.
E03 CHASSIS. SET LOSES POWER AFTER 10 MINUTES. CB500 - circuit breaker defective.

E03 CHASSIS. NO VIDEO, NO SOUND.
Shorted Q206 IF transistor.
E04 CHASSIS. NO CHANNEL 6.
SC3 diode in VHF tuner shorted.
E04 CHASSIS. SET DEAD. Open SW502.

E06 CHASSIS. LOSE PIX AND SOUND AFTER 5 MINUTES. L225 opens in Video IF.

Michael Caputo, FSDM, Levittown, Pennsylvania.

> "And to my beloved nephew, I leave the bulk of my estate: five gallons of gasoline!"

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